



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **WATANABE, Kenichi**

Serial No.: **09/987,012**

Filed: **November 13, 2001**

Group Art Unit: **2815**

Examiner: **Chris C. Chu**

P.T.O. Confirmation No.: **6363**

For: **SEMICONDUCTOR WAFER DEVICE HAVING SEPARATED  
CONDUCTIVE PATTERNS IN PERIPHERAL AREA AND ITS  
MANUFACTURING METHOD**

**AMENDMENT UNDER 37 CFR §1.111**

Commissioner for Patents  
Washington, D.C. 20231

May 15, 2003

Sir:

In response to the Office Action dated **January 15, 2003**, extended to **May 15, 2003** by a  
**one (1) month** Petition for Extension of Time, please amend the above-identified application as  
follows:

**IN THE SPECIFICATION:**

The paragraph beginning at line 22, page 5, has been rewritten as follows:

**B1**  
Figs. 8A to 8C are cross sectional views showing a modification of the embodiment shown  
in Figs. 6A to 6D.

The paragraph beginning at line 5, page 10, has been rewritten as follows:

**B2**  
Referring to Fig. 12C, in order to avoid the influence of dishing, after the second insulating  
layer 18 is formed, its surface is planarized by CMP. It is difficult to perform CMP uniformly over  
the whole wafer surface. The wafer peripheral area is likely to be polished more than the wafer

#10/B  
And.  
J. McMillan  
5/22/03

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